Development of the fast interlock system at the BigRIPS separator

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A beam interlock system is particularly important for protecting beam line devices from the failure of magnets and other devices. The failure of beam line magnets can lead to the miss-steering of the beam and the beam might hit the beam pipe or other devices mounted along the beam line. If the beam power is high, such unexpected beam irradiation can cause serious damage to devices. The ^{238}U beam with an energy of 345 MeV/nucleon and the intensity of 1 particle μA can melt stainless steel even in 1 ms if it is focused at a diameter of 2 mm. In order to prevent damage, the beam should be stopped as soon as possible. The Beam Interlock System (BIS)[1,2] is installed at RIBF for this purpose. The BIS monitors the normal operation of devices and sends a beam-stop signal to the beam chopper installed at the exit of the ion source when a device fails. The beam chopper stops the beam within a few microseconds upon receiving a stop signal. The total response time of the existing BIS is only several milliseconds since the system uses Programmable Logic Unit (PLC) as signal processing. To cope with high-power beams extracted from the Superconducting Ring Cyclotron (SRC) at RIBF, the response time of the existing interlock system is currently inadequate and hence, a new interlock system with a fast response is developed.

A prototype of the fast interlock system with 4 analog inputs and 8 logic inputs has been developed to evaluate the speed of the response. In order to achieve a fast response time, a compact RIO system (cRIO), cRIO-9075 of National Instrument Co. Ltd. is utilized as the processing unit. The cRIO consists of a CPU and a field-programmable gate array (FPGA) that are closely related to each other. The FPGA allows a fast response between the input and output and the CPU provides versatile control of the unit. A fast sampling ADC module, NI-9222 with 500 k sample/sec, is used for analog inputs, and fast digital I/O modules, NI-9401 with 100 ns propagation delay, are used for logical inputs and outputs. Fig. 1 shows the block diagram of the interlock logic. As seen in the figure, an analog input is digitized in the ADC and compared with pre-defined upper and lower limits; the fault output is produced if the digitized value exceeds those limits. The fault output is then masked with an enable/disable flag and latched in a Set-Reset flip-flop in order to hold a fault situation. A logic input is exclusive-or'ed with a polarity flag and latched in the same way. The values in the flip-flops are or'ed together to produce a failure output. These control logics are stored in the FPGA of the cRIO and executed at a fast speed. The CPU of the cRIO is used as the interface to the comprehensive control system of the BigRIPS[3] that utilizes EPICS[4] as the base. Statuses of faults and digitized values of the analog inputs are monitored by the control system of the BigRIPS. The upper and lower limit values of the analog input and input masks are dynamically set from the control system. The programming of cRIO is performed in a LabVIEW developer environment.

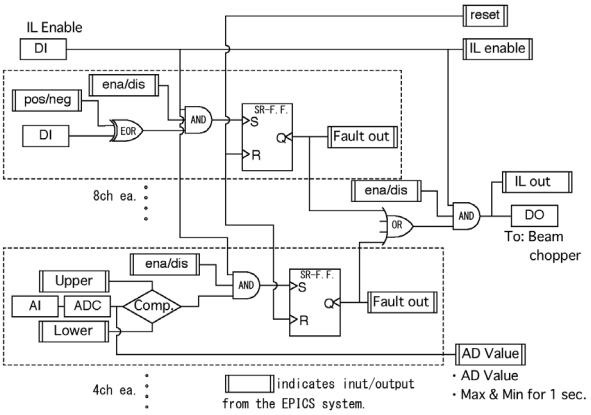

Fig. 1 Logic diagram of the prototype of the fast interlock system.

The response speed of the prototype of the fast interlock system was measured with a test signal. A step signal was inputted to the logical and analog input and the time delay between the input and output signals was measured. The response times are 0.2 μs for logical inputs and 5 μs for analog inputs. These are sufficiently fast for the fast interlock system. The prototype was also examined with the actual current monitor signal of the power supply of the first dipole magnet at BigRIPS. The current monitor signal was connected to one of the analog inputs and the digitized value was monitored. The digitized value was fluctuated within 0.25% due to the noise that appeared in the monitor signal. This is similar to the value compared with the hardware comparator built in the power supply to detect the output current drift.

Based on the successful test results on the prototype, the fast interlock system of the BigRIPS has been designed to monitor the analog and logical signals from power supplies of the 34 magnets placed at the primary beam line and the BigRIPS where a high-power primary beam is transported. The system consists of 4 cRIOs and sends the beam stop signal to the beam chopper as well as BIS. The fabrication of the system will be completed by the end of March 2014 and the system is expected to be operational by the end of July 2014.

References

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4) http://www.aps.anl.gov/epics/.

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