

Development of a prototype module for the lead-glass calorimeter readout and an ASIC for GEM foil trigger for J-PARC E16 experiment

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Development of detectors for the new spectrometer¹⁾, GEM tracker (GTR), Hadron Blind Detector (HBD) and lead-glass electromagnetic calorimeter (LG), and electronics is currently in progress.

The number of readout channels of LG is about 1100. Therefore, a dedicated and cost effective readout module has been developed in collaboration with Open-It²⁾. The specification of the prototype module is listed in Table 1 and the picture is shown in Fig. 1, which has been delivered and is currently undergoing tests. The prototype module is fabricated as the KEK-VME 6U standard. The analog input signals are split into two lines, one is fed into the comparator to generate binary outputs used for trigger primitives, and the other is followed by an analog memory. The analog memory is realized by DRS4³⁾ ASIC, which contains 1024 sampling cells per channel and can store the waveform in a gigahertz range. To extend the analog buffer, two channels are cascaded for one analog input on the prototype

Table 1. Specification of the prototype module for the LG.

parameter	value
number of analog inputs	16
analog input range	0 to -2 V
resolution	12 bit
analog memory	2048 samples / channel
readout time	30 nsec / sample
discriminator out	LVDS
readout/ slow control	TCP (100 Mbps) / UDP
power supply	± 3.3 V (KEK-VME J0 bus)

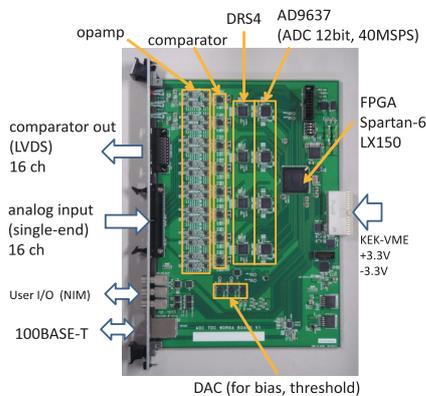


Fig. 1. A picture of the prototype module for the LG.

Table 2. Specification of the GEM trigger ASD.

parameter	value
input range	10 fC – 1 pC
shaper time constant	25 ns
pulse width	< 200 ns
conversion gain	3.0 mV/fC
ENC	20000 ($C_d = 2$ nF)
number of channel	6
power supply	± 2.5 V

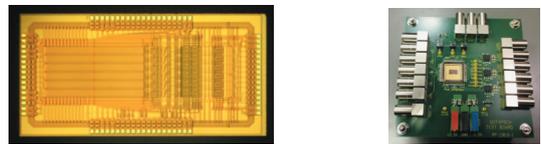


Fig. 2. Pictures of the GEM foil trigger ASIC and its evaluation board.

module. Therefore, 2 μ sec analog buffer is available if the sampling speed is set at 1 GHz, which implies that a long delay cable is unnecessary for delaying analog pulses. The waveform stored in the DRS4 is digitized by AD9637 at 33 MHz. Since the DRS4 supports a readout only in the region of interest, the dead time for an analog pulse with the width of ~ 100 nsec is expected to be less than ~ 5 μ sec. The slow control for setting a discriminator threshold and the data readout are performed by the Xilinx FPGA Spartan6-LX150 via the Ethernet.

The e^+e^- event trigger consists of three-fold coincidence of GTR, HBD, and LG. We will use a cathode plane of a GEM foil of the most outer GTR chamber. The GEM foil is divided into 24 segments. Each segment has detector capacitance of 2 nF and its hit rate is expected to be 1-2 MHz in the forward region of the spectrometer. In order to cope with such a high rate with large input capacitance in the small form factor, we have developed a new Amplifier-Shaper-Discriminator (ASD) IC with low noise and fast shaping time in collaboration with Open-It. The specification is summarized in Table 2 and the photos are shown in Fig. 2. The analog part works nearly as expected. The digital part is currently undergoing tests.

References

- 1) S. Yokkaichi *et al.*: in this report.
- 2) <http://openit.kek.jp/>
- 3) <http://www.psi.ch/drs/>

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