# Performance of scalable readout system

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The aim of the E16 experiment to be conducted at J-PARC is to study the nature of vector mesons in nuclei in order to investigate chiral symmetry restoration in dense nuclear matter[1]. A readout system is required for measuring the high rate and the large datasets. Our expected trigger rate is approximately 1 kHz, and the expected occupancy reached to be 30% at maximum.

We plan to construct a readout system for the Hadron Blind Detector (HBD) and Gas Electron Multiplier (GEM) trackers using APV Hybrid chips and Scalable Readout System (SRS) module[2]. An APV chip is an analogue pipeline ASIC[3]. The chip consists of 128 channels of preamplifiers and shapers driving a 192-column analogue memory. The SRS module is used for the slow control of APV chips, the digitization of analog data from the APV chips, and transfer of digital data to a computer using UDP/IP[4]. The SRS module has an 8-port HDMI interface to connect APV chips. Therefore, one SRS module can support 8 Master/Slave APV (16 APV chips) hybrid chips. It corresponds to $128 \times 16 = 2048$ detector outputs.

The data size of the SRS output for unit sampling time per event per channel is 2 bytes. If we take data with 27 sampling time units which is sufficient length for the E16 experiment, the entire data size per event per module is $2 \times 2048 \times 27 \sim 110$ kBytes. Since our planned trigger rate is approximately 1 kHz and the expected occupancy is 30% at maximum, the SRS module must read out and transfer data at a rate of 110 k$\times$1000 $\times$ 0.3 = 33 MBytes/s. A transfer rate of 33 MBytes/s is the requirement of the E16 experiment for evaluating the performance of the SRS module.

We discovered that the SRS module satisfied the requirement of the E16 experiment. Initially, one SRS module was connected to a computer. Four ADC channels (corresponding to 512 channels) were read out. A trigger was generated by a function generator. We measured the data transfer rate on the computer as function of trigger rate. Figure 1(a) shows the measurement results. In Fig. 1(a), the red line represents the theoretical value at the given trigger rate. Measured values are consistent with the theoretical values until the data transfer rate reaches 110 MBytes/s. The measured value dropped with the rate, 4 kHz, because a part of the trigger was injected within the dead time of the SRS module. This result satisfies the requirement of the E16 experiment. Next, two SRS modules were connected to a computer via a network switch. Then we measured the data transfer rate for this case. Figure 1(b) shows the measurement results. The Y-axis in Fig. 1(b) denotes the sum of the transfer rate. Black squires denote the results when four ADC channels were read out in both SRS modules. Red circles show the results when two ADC channels were read out in one module and six ADC channels in the other. These measured values were consistent with the theoretical values until the transfer rate sum reached 120 MBytes/s. This result supports that the network switch do not affect the data transfer rate. A single computer can handle several SRS modules. In addition, we confirmed in the same manner that the readout performance does not degrade using the zero-suppression process. Since the data transfer was carried out by using UDP, data loss may occur. Since the rate of data loss is less than once per 10 hours of operation, the efficiency of the data taking will not be affected by the rejection of the errors at the event build. Consequently, hardware performance of the SRS module satisfies the requirement of the E16 experiment.

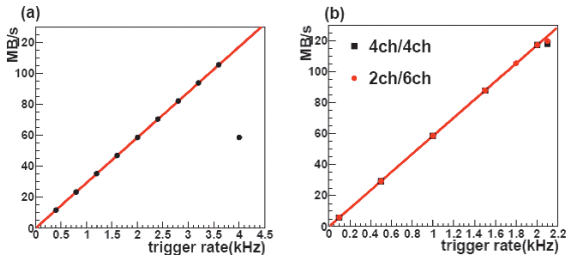


Fig. 1. Data transfer rate.(a)one SRS module. Four ADC channels were read out (b) two SRS module.Black squires show the results when 4/4 ADC channels were read out. Red circles show the results when 2/6 ADC channels were read out.

Approximately 95,000 channels must be read out via the APV chips and the SRS modules. A minimum of 780 APV chips and 49 SRS modules will be necessary. The number of SRS modules handled by one computer will be determined based on the writing speed of the disk. Since the expected occupancy will be about 10% on an average, one computer may handle 8 $\sim$ 10 SRS modules. Therefore, 5 $\sim$ 6 computers will be used for DAQ. Further, the performance study with random trigger is also in progress.

References

1) S. Yokkaichi et al. in this report.
2) S. Yokkaichi et al. , J-PARC Proposal No.16 http://j-parc.jp/researcher/Hadron/en/pac_0606/pdf/p16-Yokkaichi_2.pdf
3) https://espace.cern.ch/rd51-wg5/srs/Documentation/APV_User_Guide_2.2.pdf
4) https://espace.cern.ch/rd51-wg5/srs/Documentation/SRS_Slow_Control_Manual.pdf

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