Multiplicity trigger array for the SπRIT experiment

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In the SπRIT (SAMURAI pion Reconstruction and Ion Tracker) experiment, it is important to identify the charged pions that are generated from heavy ion collisions of high centrality and reconstruct their momenta to determine the π^+/π^- ratio, which contains information on the nuclear symmetry energy. To accumulate data that focuses on symmetry energy, it is also important for the trigger system to have sensitivity to the event centrality. As it is well known that the impact parameter correlates with multiplicity of the collision, higher-centrality collisions are extractable preferentially by triggering events with high multiplicity. While detail analysis on charged particle multiplicity will be necessary through SπRIT-TPC,[1)] the impact parameter within at least 5 fm as a central collision must be survived at the stage of triggering.

We have developed an trigger detector sensitive to multiplicity for the SπRIT-TPC data acquisition, which is called the "multiplicity trigger array". This detector consists of 30 extruded scintillator bars that are in close contact with both sides of the TPC, which is shown in Fig.1 as enclosed with an orange dotted line, using 60 bars in total. The walls of the TPC are 1mm thick aluminum windows allowing light fragment particles from the reaction to pass through and be detected by the external triggering system. The dimensions of each scintillator bar are 450 mm*50 mm*10 mm, which are coated with oxidized titanium to improve light reflection. Each bar has a hole of about 1.5 mmϕ centered along its length for a wave length shifting fiber. The collected light will be detected by 1.3 mm^2 MPPC attached to the ends of the fiber.

For readout electronics, the VME-EASIROC[2)] is used. This module was developed by Tohoku and KEK group in 2014, for the readout of multi-MPPC detector systems. EASIROC (Extended Analogue Silicon PhotoMultiplier ReadOut Chip) is used for 32 photodiodes readout developed by Omega in France.[3)] Each chip has a parallel circuit of preamplifiers, shapers, and discriminators. VME-EASIROC has two EASIROC chips on the board and is capable of reading out 64 MPPCs. The parameters of the EASIROC are variably controlled by the onboard FPGA communicating via an SiTCP connection to another computer. We can also obtain the information of the MPPC signal by the ADC onboard chip and the MHTDC logic implemented in the FPGA. The calculation logic for multiplicity is located on the FPGA, which is done by counting the number of discriminator signals that surpass the threshold value. After the calculation, the result will be compared with the user set threshold of multiplicity and generate a trigger signal within about 52 ns for the whole VME-EASIROC module.

In the fall of 2015, the SπRIT-TPC was commissioned by performing an experiment using a ^{79}Se beam impinging on Al and Sn targets. The SπRIT-TPC was setup outside the SAMURAI magnet and surrounded by the multiplicity trigger array. The histogram in Fig.2 shows charged particle multiplicity with the condition of coincidence between at least one hit in the multiplicity trigger array and the beam start counter located just upstream of the TPC. It is clear that most of the events had low multiplicity originating due to non-central collisions. In perspective of the real experiment, analyzing commissioning data is crucial to find the optimal trigger conditions for rejecting peripheral-type collisions.[4)]

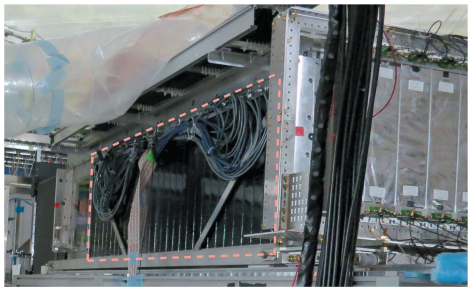

Fig. 1. One-sided view of multiplicity trigger array.

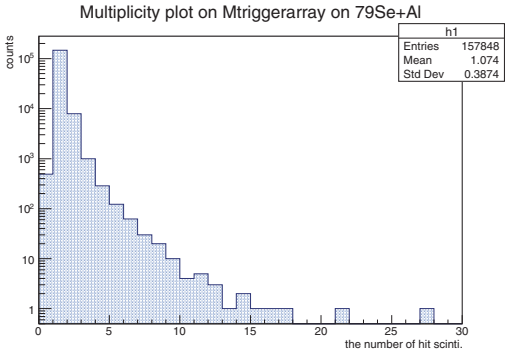

Fig. 2. Multiplicity plot of charged particle detected by multiplicity trigger array in the ^{79}Se commissioning run.

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References
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