R&D of silicon strip detector for the sPHENIX tracker

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The sPHENIX detector is a major upgrade to the PHENIX detector at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory (BNL) and is designed for exploring a vast range of physics areas including heavy quarkonia suppression via the three ϒ states and tagging of charm and beauty jets[1]. A precision tracking detector inside the 1.5 T BaBar superconducting solenoid, as well as a silicon vertex detector currently operated in PHENIX, play a crucial role in reducing fake track contributions and improving the momentum resolution, leading to the separation of the three ϒ states and to the separation of charm and bottom quarks[2]. In this report, we will discuss the design, technology choices, and R&D status of the prototype sPHENIX silicon tracker with a special emphasis on the high-density integrated (HDI) circuit and modularized silicon sensors.

The HDI circuit connects the readout chips to the downstream frontend boards, and custom 128-channel front-end ASIC 'FPHX'[3] chips are planned. The design of the HDI has taken into account (1) the effects of both common-mode and differential-mode noise, (2) the desire to minimize the geometrical size, and (3) the desire to limit the material budget. For the first point, the HDI design for the silicon tracker follows the PHENIX-FVTX design that is coupled to the FPHX chips and copes with the effects of both common-mode and differential-mode noise by surrounding the signal layers by the grounding layers[4]. The second point is very important for the silicon tracker S0 and S1 stations (see the other Reports[2] for details), as they must be made compact for installation in a tiny space relative to the S2 station. The third point is especially important for the S1 station, where the effects of multiple scattering are most significant and thus may cause poor momentum resolution.

Considering the requirements listed above, we started the HDI R&D by placing a higher priority on the S0 and S1 stations compared with the S2 station. The current design of the HDI for the S1 station has seven layers of flexible printed circuits and has dimensions of 28 mm (W) × 500 m (H). The length of the HDI in the beam direction varies from 10 cm to 40 cm. The size of the HDI is well below the geometrical requirements. The prototype HDI has a thickness of approximately 0.5 % of a radiation length on average. The seven layers of flexible printed circuits have been designed with a special emphasis on the reduction of any unwanted microstrip antenna and on good impedance matching even at a distance of ∼ 40 cm from the FPHX chip. The prototype HDIs for the S1 station will be produced by Yamashita Materials Corporation and will be ready for further assembly in early 2016. Figure 1 shows the layout of the HDIs for the S1 station.

One silicon sensor, two HDIs with ten FPHX chips for each, and one CFRP support frame are assembled into a silicon sensor module as shown in Fig. 2. Because of the readout structure of the silicon sensors, the HDIs are glued onto both ends of the silicon sensors. In order to reduce the amount of material used, the two HDIs are completely separated and not connected.

In the assembly, the bonding of the FPHX chips to the silicon sensor and their attachment to the two HDIs are being performed as well. Hayashi watch-works Co., Ltd, which has experience producing the PHENIX VTX pixel detectors, will be employed for the assembly of the prototype module.

The first prototype module for the S1 station will be tested at RIKEN and BNL. The sPHENIX silicon outer tracker uses essentially the same electronics as the PHENIX FVTX detector, namely the FPHX chip and frontend circuits. The test bench at RIKEN that was originally set up for the high-multiplicity trigger development for the FVTX detectors can be applied again to test prototype sensor modules, with minor modifications in the readout configuration. The test is planned for 2016 spring and summer.

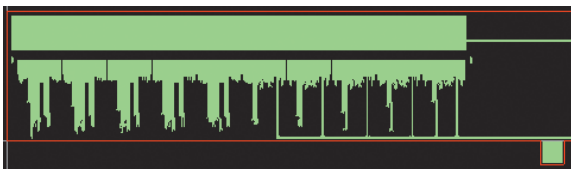

Fig. 1. Layout of the HDIs for the S1 station. The green area indicates the analog and digital circuits.

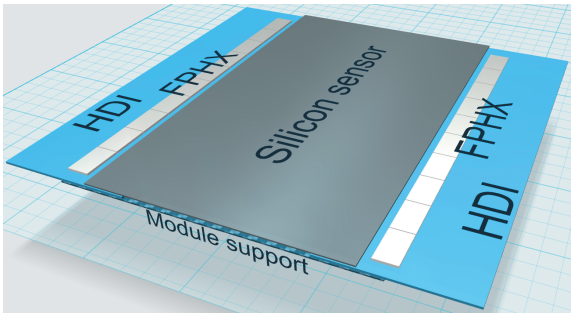

Fig. 2. CAD drawing for the silicon sensor module for the S1 station.

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