# New functions in Generic Trigger Operator

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The Generic Trigger Operator (GTO) module[1] is a field-programmable gate array (FPGA)-based NIM logic module. Common trigger firmware[2] manages trigger generation to ensure event synchronization between multiple CAMAC and VME front-end systems. GTO modules implementing this firmware are permanently installed at experiments of BigRIPS, SHARAQ, EURICA, SUNFLOWER, SAMURAI, and R3. Recently, advanced functions of scaler, gate-and-delay generator (GG) and selector have been developed for GTO. Here, we report these new functions.

**Scaler**

The scaler function has been introduced in the GTO module. Scaler values can be readout via the Ethernet. The functionality of the scaler firmware is as follows.

- 20-channel scaler inputs : Each scaler has a 32-bit counter depth.
- Gate input : When the gate input function is enabled, scaler circuits count up only when the gate signal is issued.
- Veto input : Inhibit counting.
- Read latch input : The readout value is held by the read latch signal. Scaler circuits are still operational even if the read latch is issued.
- Clear input : Clear the scaler values to zero.

As additional functions, 1-Hz/1-kHz/10-kHz clock signals and level/pulse signals can be output.

**Gate-and-Delay Generator**

The firmware of the 4-channel GG has been developed. Two different GG functions are introduced: clock-asynchronous and clock-synchronous GG. The clock-asynchronous GG is based on the D-Flip Flop delay chain (details are described in Ref. 1). The gate and delay circuits are driven according to the leading edge of the input signal. The clock-synchronous GG is implemented by simply counting up the clock signal. In this case, input signals are synchronized by the internal clock. The specification of each GG function is described bellow.

- clock-asynchronous GG
  - Gate-width range : $T_{wid}$ = 51 ns to 2.6 ms.
  - Delay range : $T_{dl}$ = 51 ns to 2.6 ms.
  - Minimum step of $T_{wid}$ and $T_{dl}$ : 1.2 ns.
  - Timing jitter : $\sigma \simeq T_{dl} \times 10^{-4}$.

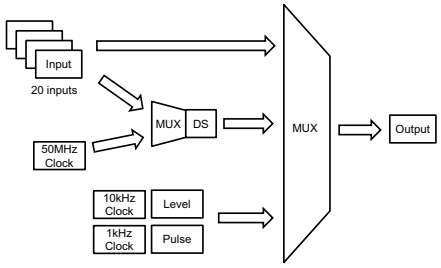


Fig. 1. Functional diagram of the selector firmware

- clock-synchronous GG
  - Clock interval : $T_{int}$ = 20 ns to 10 $\mu$s.
  - Gate-width range : $T_{wid}$ = 20 ns to 171 s.
  - Delay range : $T_{dl}$ = 20 ns to 171 s.
  - Timing jitter : $\sigma = T_{int}/2\sqrt{3}$ .

In the case of the clock-synchronous GG, the clock signal is variable. The minimum clock interval ($T_{int}$) is 20 ns, which originates from a 50-MHz crystal resonator. This clock can be divided into 1/1 to 1/256 frequency in FPGA. Thus, the clock interval is varied between 20 ns and 10 $\mu$s. The timing jitter of the output signal in clock-synchronous GG depends on $T_{int}$ because deterministic jitter is generated when the input signal is synchronized by the clock. On the other hand, the timing jitter in clock-asynchronous GG is a random jitter.

**Selector**

A selector firmware has been developed to remotely switch signal sources. The functional diagram is shown in Fig. 1. There are 8 output channels. Each output channel can be chosen from signal sources by the multiplexer (MUX) circuit. The signal sources of the 20 inputs, down scaler (DS), 1k/10k-Hz clock, pulse, and level signals are available. Input signals and 50-MHz clock signals can be decimated using the DS circuit: this function is the so-called rate divider or down scaler.

These new functions implemented as firmware are utilized in RIBF experiments. In addition, the development of the time-to-digital converter (TDC) in the GTO is examined. The details of the TDC firmware are described in Ref 3.

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References
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