Evaluation of single event transient error rate related to operation frequency on 64bit SOI micro processor

A. Maru,[*1] K. Sakamoto,[*1] H. Shindou,[*1] S. Kuboyama,[*1] and K. Suzuki[*1]

Silicon on Insulator (SOI) devices are the focus for recent electronic applications due to their excellent characteristics which are low power consumption and possibility of miniaturization. They also have excellent characteristics with regard to the angle of radiation tolerance. Single event latch up (SEL) has never occurred in SOI devices due to their cross-sectional structure. Since the SOI transistor has been electrically isolated from others by buried oxide (BOX), electrical circuits with excellent single event upset (SEU) and single event transient (SET) tolerance can be composed by using SOI transistors. In addition, the Japan Aerospace Exploration Agency (JAXA) focused on SOI devices for space applications and has been continuously involved in research and development since 2005. JAXA has developed the Micro Processer Unit (MPU) and Application Specific Integrated Circuit (ASIC) for space applications by combining SOI devices and radiation hardness by design (RHBD) techniques.[1)] They are used in numerous spacecraft. Recently, it was reported in certain project that many SEUs were observed in the SOI product used in satellites. Reported error rates of SEUs on the orbit was higher than the calculated error rates from radiation tests on the ground. Therefore, it was suggested that some defects exist in this device.

From our analysis, it was identified that one defect in this device was due to a parasitic diode on the drain area of the SOI transistor, as shown in Fig.1. We identified the parasitic diode was created in one fabrication process of the SOI transistor, so we tried to fix this defect by changing the process condition of the SOI transistor. The evaluation results of the SOI device, which was fabricated using a fixed process condition indicated that it had high radiation tolerance. Under static test conditions, no error was observed on this device. However, a few errors were observed under dynamic test conditions (continuous memory data read/write condition). It is presumed that the cause of this error is temporal read miss due to SET.

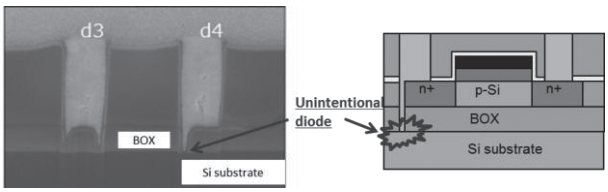

Fig. 1. Cross-sectional structure image of SOI transistor with unintentionally formed parasitic diode.

[*1] Japan Aerospace Exploration Agency

In the case of error due to SET, the error rate depends on the operation frequency of the device. Therefore we evaluated the error rate operation frequency dependence of this SOI device for calculating the error rate on the orbit.

The test sample was irradiated with a Kr-ion beam of 713 MeV using the RIKEN RILAC+RRC. Total fluence was set to 5×10^{7} ~ 1×10^{8} ions/cm^{2} at the chip surface. The operation frequency of the device was set to 0.5, 5, 50 MHz. The irradiation test was performed under dynamic test conditions.

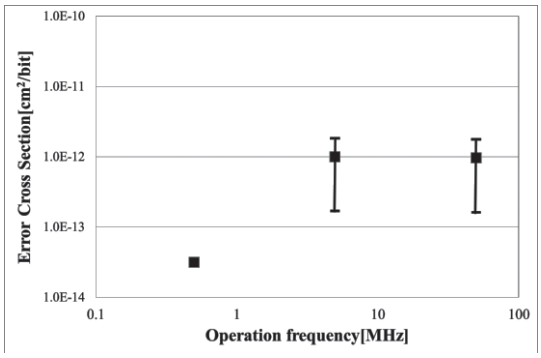

Fig. 2. SOI device irradiation test result under a dynamic test condition.

Figure 2 shows the data of error cross section which depends on operation frequency. The operation frequency dependence was not observed within the uncertainty of the data. Note that the value of error cross section is extremely low, so this error seldom occurs. Based on the evaluation results of error cross section, the calculated error rate on the orbit can be almost ignored.

The SOI device which was fabricated using the fixed process condition, indicated excellent radiation tolerance. We confirmed that the error rate on the orbit of this device can be almost ignored because the SET error cross section value is extremely low. Operation frequency dependence of SET error cross section could not be observed clearly, so we will evaluate this device with a wider frequency range in future work.

Reference

1) A. Makihara et al., RADECS, Vol.1 (2011), 164-168.