Development of a machine protection beam interlock system for the RIBF

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We started the development of a successor system to the existing machine protection beam interlock system (BIS) (hereafter, new BIS). The new BIS is based on CompactRIO,[1)] a product by National Instruments. Its prototype, consisting of two stations for digital input (DI) signals, was installed on a trial basis in parallel with the RIBF-BIS, one of the existing BIS systems, which covers the high-energy part of RIBF. The prototype worked properly during its test operation. In 2023, we improved the interlock logic of the prototype to the level of an actual system and expanded the prototype.

At first, we reconsidered the processing of the terminals for connecting input signals. The new BIS basically follows the logic of the existing BIS,[2)] which has been in operation for 17 years. Thus, upon receiving an alert signal, the new BIS outputs a signal to one of the beam choppers, which immediately deflects the beam downstream of the ion source (the time required for this is called the system response time). In addition, it inserts a beam stopper (a Faraday cup, hereafter, FC) installed upstream of the problematic component. In the BIS, the FC to be inserted is selected from the graphical user interface (GUI) for setting the conditions for each input signal contact before accelerating the beam for each experiment. In contrast, in the prototype, to make the interlock logic compact and save the use of a field-programmable gate array (FPGA) resource, all contacts and FCs are linked in advance instead of selecting them from the GUI. However, this specification has the disadvantage that the number of contacts corresponding to each FC will be limited. Therefore, we developed the same logic of the BIS for the prototype, and compared the FPGA resource usage and system response time. The results showed that either logic implementation could connect up to 192 DI signals to one station, and the difference in system response time between the two logics was sufficiently small to be negligible (approximately 6 μs). Therefore, we decided to apply the same logic of the BIS on the new BIS. The number of DI signals per station in the new BIS was unified to 192, more than double the current number, for all on-site stations to allow for future expansion.

The second step was to develop the processing of analog input (AI) signals. In the BIS, DI and AI signals are mixed in one station, which increases the logic processing and is thought to lead to delays in the system response time. Therefore, in the new BIS, a station for AI signals (hereafter, AI station) was constructed separately from the station for

DI signals (hereafter, DI station) based on CompactRIO, and the output signal of the AI station was wired as the input signal of the DI station. The logic to recognize each input signal as an abnormal event based on the signal mask status and signal duration of each AI signal is the same as that used for DI signals to simplify the system logic management. In the BIS, the maximum number of AI signals for one station is 40; however it will be unified to 64 for all stations in the new BIS.

In parallel with the above, we designed and built terminal boards for the new BIS based on the terminal board used in AVF-BIS to rack-mount the prototype that had been temporarily installed in a test barracks, and we also realized all the assembly and on-site wiring ourselves. In addition, the GUI for setting the specifications of the input signal condition and monitoring the signals developed for the prototype and logging system was expanded.

After completing the previous steps, we expanded the prototype installed in parallel with the RIBF-BIS station-2 by installing an additional DI station and an AI station during the summer maintenance period of 2023. By devising the logic to shorten the system response time as much as possible and adding a pull-up circuit at each DI signal contact, the system response time was 120–130 μs and approximately 470 μs to a DI signal and an AI signal input, respectively. This is sufficiently fast to meet the development target of 1 ms for the new BIS, and is approximately 100 times faster than that of the existing BIS, especially for DI signals (the average system response time for the BIS

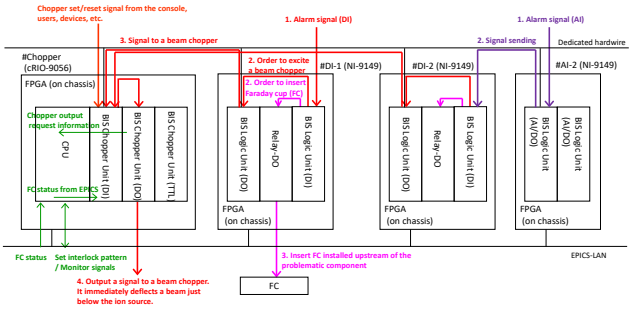

Fig. 1. Hardware configuration and process flow in the new BIS as of 2023.

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is approximately 15 ms). We started the actual operation test of the new BIS during the beam service times scheduled in the second half of the fiscal year 2023. The system is targeted for completion in FY2025.

References

1) CompactRIO, `https://www.ni.com/ja-jp/shop/compactrio.html`.
2) M. Komiyama *et al.*, RIKEN Accel. Prog. Rep. **39**, 239 (2006).