DAQ upgrade of the J-PARC E16 experiment in 2023–2024

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We proposed the experiment J-PARC E16[1,2)] to measure the vector meson decays in nuclei to investigate the chiral symmetry restoration in dense nuclear matter. The experiment started at the J-PARC Hadron Experimental Facility in 2020.

Unexpected beam microstructures were found in the commissioning run in 2021.[2)] As a countermeasure, a DAQ upgrade was planned.

GEM detectors in E16 are read out using the SRS-ATCA,[3)] which is a system originally developed to read-out micropattern gas detectors (MPGD) by the CERN/RD51 collaboration. In the E16 DAQ system, the longest busy was issued by SRS-ATCA, the typical value was 800 μs, which was governed by the data transfer time from SRS-ATCA to the data storage PC.

If the beam is uniform, trigger requests follow a uniform probability and are described by a Poisson process. In this case, the DAQ live time r_{live}, defined as the ratio of the number of accepted and requested triggers per unit time, is calculated as

$$r_{\mathrm{live}} = \frac{1}{1 + f_{\mathrm{request}} \times t_{\mathrm{busy}}},$$

where f_{request} and t_{busy} represent the average trigger request rate [Hz] and busy length [s], respectively. When the average busy length is 800 μs and the average trigger request rate is 1 kHz, the expected accept rate is $\sim$56%. However, the low live time measured in 2021 was 15%, which results from instantaneous high-rate attributed to the beam microstructure. A simulation indicated that if the busy length is reduced to below 100 μs, data acquisition would be possible at 2 kHz with around 70% live time even under the microstructure conditions. Based on this, a measure was taken to reduce the busy length.

Two options were proposed to reduce the busy length: (1) An upgrade of the network connection between the SRS-ATCA and data collection personal computer. While the SFP+ for 10G ethernet is available for the data transfer board in the SRS-ATCA system, only 1G ethernet function is implemented in the FPGA. (2) Utilizing the on-board RAM (2 GB) for the data-buffering before the data transfer from SRS-ATCA. Both can reduce the event-by-event busy length governed by the network transfer performance. The latter option was selected considering development time.

The data buffering function addresses sudden increases in trigger requests without changing the data transfer path or receiving system. Previously, FPGA memory limits led to network bottlenecks at high trigger rates; however, the data buffer before network transfer resolved this issue. Further, the function enables spill-off data transfer, which doubles the data acquisition capacity in the J-PARC beamline, where the spill cycles are about every 2 s. The main FPGA of SRS-ATCA is the XC6VLX130T. The RAM interface in the firmware is implemented using the IP core of AMD.

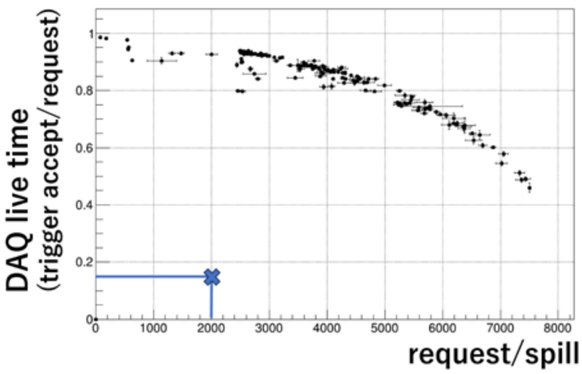

Fig. 1. Achieved DAQ live time in the 2024 beam time as a function of the request rate of the ee-trigger per beam spill. The spill length is 2 s; and therefore, "5000" in the abscissa corresponds to the trigger rate of 2.5 kHz. The blue cross corresponds to 15% for 1 kHz, which is the typical value in 2021.

In June 2023, a short beam time was available and the first version of the system was tested successfully, using the minimum-bias trigger, which was $\sim$1 hour of beam time. In May 2024, the system was operated for the ee-trigger, which is the main trigger of the E16 experiment. The achieved performance is depicted in Fig. 1. Typical live times in the ee-trigger were 82 and 94% at 2.5 and 1.2 kHz, respectively. The trigger rate values vary with the beam conditions, and therefore, we configure the trigger rate within this range. For the 2.5 kHz trigger, the equation predicts a busy length of 84 μs at an 82% live time, while the measured value was 52 μs. Similarly, for the 1.2 kHz trigger, the calculated busy length at 94% live time was 53 μs, whereas the measured value was 34 μs. These discrepancies originate from the microstructure effects.

The performance is sufficient for the E16 physics run, and the system will be operated in the upcoming physics run.

References
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