Improvement of single-event burnout tolerance in SiC power devices†

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Single-event burnout (SEB) is a catastrophic failure of power devices triggered by heavy-ion irradiation. Power devices are used in spacecraft power supply components, and therefore, SEB can directly lead to the loss of spacecraft. Therefore, enhancing the radiation tolerance of power devices is crucial for space applications. Silicon carbide (SiC) devices exhibit SEB failure under radiation environments similar to Si devices;[1,2] however, its mechanism is debatable. Several studies suggest that adopting a buffer layer at the drift/substrate interface can effectively prevent SEB in SiC devices, similar to its effectiveness in Si devices.[3] Although this approach has shown promise in simulations, its effectiveness is yet to be validated through experimental research. In this study, we simulated and demonstrated the effect of the electric field relaxation layer at drift/substrate interface to improve SEB tolerance in N-channel trench gate SiC-MOSFETs.

Figure 1 shows the cross-sections of the fabricated 1.2 kV class N-channel trench gate SiC-MOSFETs. Figures 1(a) and (b) show the cross-sections of a typical trench gate SiC-MOSFET (Type A) and that of one with an electric field relaxation layer (Type B), respectively. The test devices were irradiated with ^{84}Kr ions at a normal incidence in air using RIKEN azimuthally varying field cyclotron in combination with the RIKEN ring cyclotron. The energy of the ion at the incident edge of the device, calculated by SRIM, was 3118 MeV, and its range was 416 μm in SiC. The fluence of the ions at each voltage step was adjusted to $\sim 3.0 \times 10^5$ cm^{-2}. The drain and gate leakage currents (I_D and I_G) were continuously monitored during irradiation. The gate-source voltage (V_{GS}) was set to 0 V.

The drain-source applied voltage (V_{DS}) started at 100 V and was increased in 100 V steps up to ID over 1 mA. The final V_{DS} is defined as the SEB voltage in this study.

Figure 2 shows the simulated depth profile of the electric field. In Type A, the electric field at the drift and substrate interface increases due to the Kirk effect, whereas the electric field at the drift and substrate interface reduces in Type B. This result implies that the electric field is relaxed by penetrating the buffer layer. Figure 3 shows the experimental results of the leakage current transition at the end of each voltage step for types A and B. Significant differences were observed between Types A and B, with the SEB voltage for Type B being 200 V higher than that for Type A. This result implies that SEB tolerance could be improved because of the electric field relaxation effect.

In conclusion, our study demonstrated that electric field relaxation achieved by adding a buffer layer is an effective approach against SEB in trench gate SiC-MOSFETs.

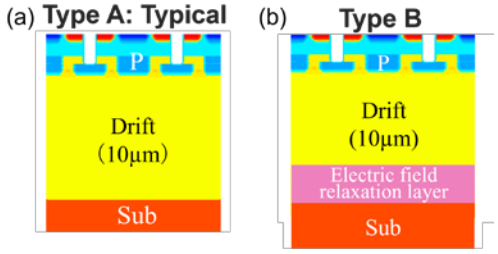

Fig. 1. Schematic cross-sectional image of trench gate SiC-MOSFETs. (a) Typical type. (b) With a buffer layer that has an electric field relaxation effect.

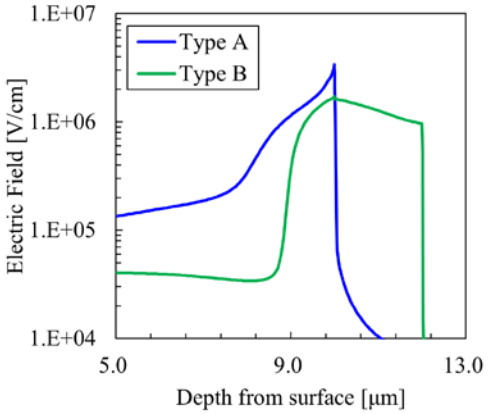

Fig. 2. Simulation results of the depth profiles of the electric field.

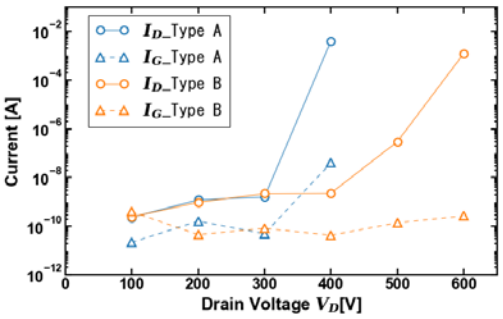

Fig. 3. I_D and I_G characteristics during irradiation.

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