Introducing EtherNet/IP to the RIBF control system: Development and operational use

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The goal of the next phase of the RIBF project is to enhance the accelerator facility by implementing a charge stripper ring (CSR).[1] The control system for the next RIBF phase should be designed to reduce development effort by leveraging commercially available hardware and open-source software wherever possible. Currently, the RIBF control system employs numerous TCP/IP-based devices interfaced with the EPICS control framework. These devices include not only commercially available devices but also custom-designed and developed devices by the Nishina Center.

In such cases, TCP/IP-based devices and EPICS input/output controllers (IOCs) communicate by exchanging commands through socket communication. However, unexpected power failures in devices or network switches can cause critical losses of socket communication. Under these circumstances, reconnection between the EPICS IOC and the devices may not be possible.

To address these issues, the CSR control devices should introduce reliable Ethernet-based field networks such as EtherCAT and EtherNet/IP, which are highly useful at the device interface layer instead of TCP/IP. Before the implementation in the next phase, we introduced field networks at the device interface layer within the existing accelerator facility to evaluate their utility. As part of this effort, we replaced the TCP/IP-based device known as N-DIM[2] with an EtherNet/IP-based device.

N-DIM, designed and developed at the Nishina Center, is a device equipped with 32-channel digital inputs, 32-channel digital outputs, and 16-channel analog inputs. The device communicates with the EPICS IOC via TCP/IP and can be used for general purposes such as beam diagnostic equipment, vacuum control panels, and magnet power supply control. As the first step, we developed a device using EtherNet/IP to replace the N-DIM used for controlling the Faraday cup (FC), which is a beam diagnostic instrument at RILAC. The newly developed device, with functionality compatible with N-DIM excluding analog inputs, was constructed using the FA-M3 programmable logic controller (PLC).

EtherNet/IP-based systems comprise a scanner and adapters. In the system designed for FC control, the scanner resides on the EPICS IOC side, while the device functions as the adapter. The scanner is implemented on the F3SP71 sequence central processing unit (CPU) installed in the first slot, which provide interlock functionality. Meanwhile, the high-level application interface for EPICS is implemented on the Linux CPU

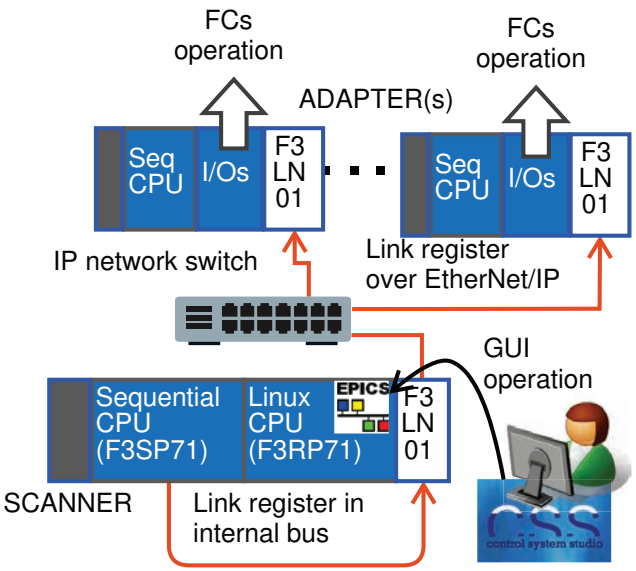

Fig. 1. EtherNet/IP is provided by F3LN01 which is dedicated module. The scanner, an EPICS IOC, achieves highly reliable communication with multiple adapters despite using a general-purpose network.

F3RP71-1R installed in the second slot, which forms a multi-CPU configuration. When handling EtherNet/IP in the FA-M3 PLC system, the I/O exchange between adapters and scanners is expressed as standard link registers (W registers). Therefore, developers can create programs based on these link registers without dealing directly with the EtherNet/IP protocol, which allows them to follow standard FA-M3 PLC system development practices, which helps realize low development costs. Consequently, EtherNet/IP successfully provides a cost-effective and highly reliable mechanism for data exchange between EPICS IOCs and devices (see Fig. 1).

The newly developed device served as an EtherNet/IP adapter, which acted as a replacement for two N-DIM units and up to four FCs. Ultimately, a total of six adapters were installed for one scanner in the RILAC control system. The replacement was conducted during the summer maintenance period, and since then it has successfully supported subsequent accelerator operations and supplied the beam to experimental courses without any issues.[3] In future, we plan to consider replacing aging devices for magnet power supplies with EtherNet/IP-based devices.[4]

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References

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